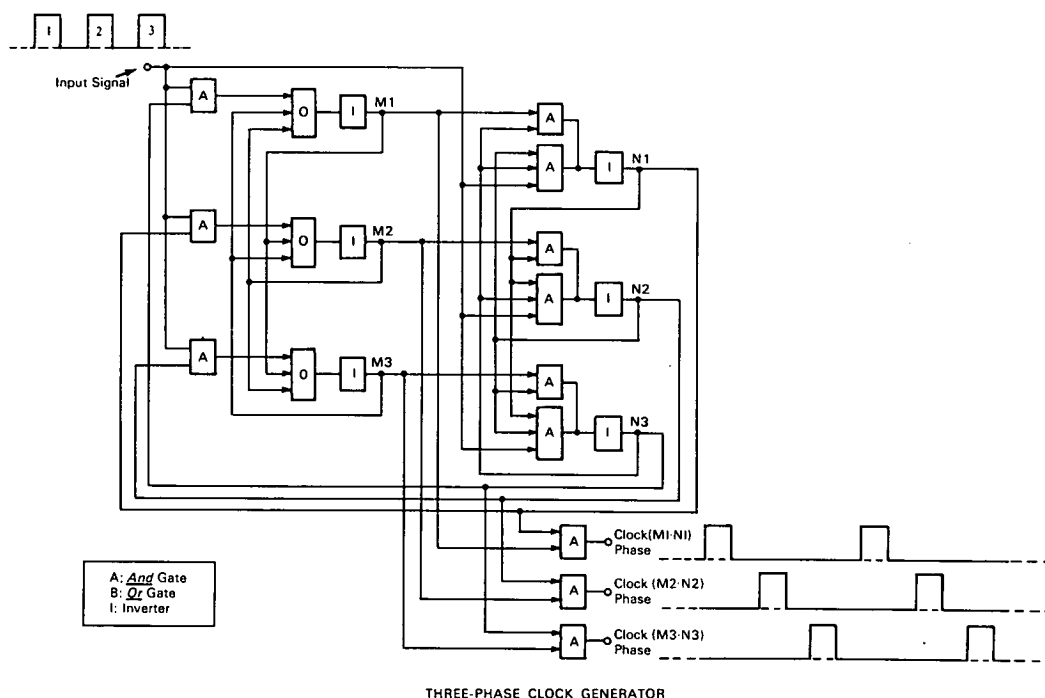


NASA TECH BRIEF



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Multiphase Clock-Pulse Generator Uses Simplified Circuitry



The problem: To simplify multiphase clock-pulse generators required in most electronic pulse and digital logic systems. These clock-pulse generators have used relatively complex circuitry to avoid logical situations in which extraneous pulses might be formed.

The solution: A multiphase clock-pulse generator that converts a simple pulse train into nonoverlapping clock pulses. The generator employs multistable circuits, incorporating *and* gates, *or* gates, and inverters, to minimize the number of electronic components.

How it's done: The block diagram presents a three-phase clock-pulse generator to illustrate the operating principle of the multiphase system. The three-phase generator employs two tristable circuits interconnected to three output *and* gates which provide the clock pulses.

Each of the three stages of the first tristable circuit consists of an *and* gate, an *or* gate, and an inverter which are interconnected so that only one stage at a time can be at the up-level (1-state). For example, the respective outputs M1, M2, and M3 of this tristable circuit are initially in the 0, 0, 1 state. The second

(continued overleaf)

tristable circuit has outputs N1, N2, and N3. Each of the three stages of this circuit consists of two *and* gates coupled to an inverter, and only one stage at a time can be at the down-level (0-state).

The first tristable circuit changes state when the input signal is at an up-level. The second tristable circuit changes state when this signal is at a down-level. The state assumed by the first tristable circuit when the input is up-level depends on the state last stored in the second tristable circuit. The state assumed by the second tristable circuit when the input is down-level depends on the state last stored in the first tristable circuit. This interdependency between the tristable circuits is achieved by interconnections that allow the stages to advance through all states in an interleaved succession and then repeat. The three-phase clock signal is obtained by *and* gating M1 with N1, M2 with N2, and M3 with N3, respectively.

Notes:

1. The basic three-phase generator can be expanded to provide a multiphase (n-phase) clock output. In the n-phase generator, the first multistable circuit would have n stages and an initial condition of 0, 0, 0, . . . 0, 1. The second multistable circuit would also have n stages, but an initial condition of 1, 1, 1, . . . 1, 0. The nth-phase clock signal would be obtained by *and* gating Mn with Nn.
2. This type of generator should find application in pulse, digital, and pulse-coded electronic systems.
3. Inquiries concerning this invention may be directed to:

Technology Utilization Officer
Marshall Space Flight Center
Huntsville, Alabama, 35812
Reference: B65-10353

Patent status: NASA encourages the immediate commercial use of this invention. Inquiries about obtaining rights for its commercial use may be made to NASA, Code AGP, Washington, D.C., 20546.

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